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ENTITLED

PLATED TERMINATIONS

BY

ANDREW P. RITTER

ROBERT HEISTAND II

JOHN L. GALVAGNI

AND

SRIRAM DATTAGURU

PATENT

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TITLE: PLATED TERMINATIONS

PRIORITY CLAIMS

This application claims the benefit of priority as a continuation-in-part application of previously filed U.S. Utility Patent Application entitled "PLATED TERMINATIONS", filed April 8, 2003 and assigned USSN 10/409,023, which application respectively claims priority to U.S. Provisional Patent Application entitled "PLATED TERMINATIONS," filed April 15, 2002 and assigned USSN 60/372,673, and which are incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

The present subject matter generally concerns improved termination features for multilayer electronic components, and more particularly relates to plated terminations for multilayer electronic components, such as capacitors, resistors, etc. or for integrated passive components. The subject termination design utilizes selective arrangements of internal and/or external electrode tabs to facilitate the formation of plated electrical connections. The external connections are preferably made whereby the provision of typical thick film termination stripes is eliminated or greatly simplified.

Many modern electronic components are packaged as monolithic devices, and may comprise a single component or multiple components within a single chip package. One specific

example of such a monolithic device is a multilayer capacitor or capacitor array, and of particular interest with respect to the disclosed technology are multilayer capacitors with interdigitated internal electrode layers and corresponding electrode tabs. Examples of multilayer capacitors that include features of interdigitated capacitor (IDC) technology can be found in U.S. Patent Nos. 5,880,925 (DuPré et al.) and 6,243,253 B1 (DuPré et al.). Other monolithic electronic components correspond to devices that integrate multiple passive components into a single chip structure. Such an integrated passive component may provide a selected combination of resistors, capacitors, inductors and/or other passive components that are formed in a multilayered configuration and packaged as a monolithic electronic device.

Selective terminations are often required to form electrical connections for various monolithic electronic components. Multiple terminations are needed to provide electrical connections to the different electronic components of an integrated monolithic device. Multiple terminations are also often used in conjunction with IDC's and other multilayer arrays in order to reduce undesirable inductance levels. One exemplary way that multiple terminations have been formed in multilayer components is by drilling vias through selected areas of a chip structure and filling the vias with conductive material such that an electrical connection is formed among selected electrode portions of the device.

Another way of forming external terminations for the subject devices is to apply a thick film stripe of silver or copper in a glass matrix to exposed portions of internal electrode layers, and subsequently plating additional layers of metal over the termination stripes such that a part is solderable to a substrate. An example of an electronic

component with external electrodes formed by baked terminations and metal films plated thereon is disclosed in U.S. Patent No. 5,021,921 (Sano et al.). The application of terminations is often hard to control and can become problematic with reduction in chip sizes. U.S. Patent Nos. 6,232,144 B1 (McLoughlin) and 6,214,685 B1 (Clinton et al.) concern methods for forming terminations on selected regions of an electronic device.

The ever-shrinking size of electronic components makes it quite difficult to print termination stripes in a predetermined area with required precision. Thick film termination stripes are typically applied with a machine that grabs a chip and applies selective terminations with specially designed wheels. U.S. Patent Nos. 5,944,897 (Braden), 5,863,331 (Braden et al.), 5,753,299 (Garcia et al.), and 5,226,382 (Braden) disclose mechanical features and steps related to the application of termination stripes to a chip structure. Reduced component size or an increased number of termination contacts for an electronic chip device may cause the resolution limits of typical termination machines to become maxed out.

Other problems that can arise when trying to apply selective terminations include shifting of the termination lands, mispositioning of terminations such that internal electrode tabs are exposed or missed entirely, and missing wrap-around termination portions. Yet further problems may be caused when too thin a coating of the paint-like termination material is applied or when one portion of termination coating smears into another causing shorted termination lands. These and other concerns surrounding the provision of electrical termination for monolithic devices create a need to provide cheap and effective termination features for electronic chip components.

In light of component miniaturization and concerns with providing terminations that do not short together, especially

when positioning multiple components in proximity on a circuit board, U.S. Patent No. 6,380,619 (Ahiko et al.) provides a chip type electronic component having external electrodes that are spaced at predetermined distances from side surfaces of a ceramic substrate. More particularly, electronic components having three-sided terminations as opposed to more conventional five-sided terminations are disclosed. Such components with three-sided terminations are more easily provided in an adjacent relationship with one another without shorting together distinct component terminations. Some embodiments disclosed in Ahiko et al. include electroplated films applied to the exposed portions of individual electrodes.

Yet another known option related to termination application involves aligning a plurality of individual substrate components to a shadow mask. Parts can be loaded into a particularly designed fixture, such as that disclosed in U.S. Patent No. 4,919,076 (Lutz et al.), and then sputtered through a mask element. This is typically a very expensive manufacturing process, and thus other effective yet more cost efficient termination provisions may be desirable.

U.S. Patent Nos. 5,880,011 (Zablotny et al.), 5,770,476 (Stone), 6,141,846 (Miki), and 3,258,898 (Garibotti), respectively deal with aspects of the formation of terminations for various electronic components.

Additional background references that address methodology for forming multilayer ceramic devices include U.S. Patent Nos. 4,811,164 (Ling et al.), 4,266,265 (Maher), 4,241,378 (Dorrian), and 3,988,498 (Maher).

While various aspects and alternative features are known in the field of electronic components and terminations therefor, no one design has emerged that generally addresses all of the issues as discussed herein. The disclosures of all the

foregoing United States patents are hereby fully incorporated into this application by reference thereto.

BRIEF SUMMARY OF THE INVENTION

The present subject matter recognizes and addresses various of the foregoing shortcomings, and others concerning certain aspects of electrical terminations and related technology. Thus, broadly speaking, a principal object of the presently disclosed technology is improved termination features for electronic components. More particularly, the disclosed termination features are plated and designed to eliminate or greatly simplify thick-film stripes that are typically printed along portions of a monolithic device for termination purposes.

Another principal object of the presently disclosed technology is to offer a way to guide the formation of plated terminations through the provision of internal electrode tabs and the optional placement of additional anchor tabs. Both internal electrode tabs and additional anchor tabs can facilitate the formation of secure and reliable external plating. Anchor tabs, which typically provide no internal electrical connections, may be provided for enhanced external termination connectivity, better mechanical integrity and deposition of plating materials.

Yet another principal object of the present subject matter is to provide termination features for electronic components whereby typical thick-film termination stripes are eliminated or simplified, and only plated terminations are needed to effect an external electrode connection. Plated materials in accordance with the disclosed technology may comprise metallic conductors, resistive materials, and/or semi-conductive materials.

A still further principal object of the subject termination technology is that termination features can be used in

accordance with a variety of multilayer monolithic devices, including, for example, low inductance ceramic capacitors and capacitor arrays, multilayer ceramic capacitors and capacitor arrays, and integrated passive components. Integrated passive components may include a select combination of resistors, capacitors, varistors, inductors, baluns, couplers, and/or other passive components.

A resultant advantage of the disclosed subject matter is that termination features for electronic components can be effected without the need for application by termination machinery, thus providing an ability to yield external terminations with resolution levels that may otherwise be unattainable. Such improved termination resolution also enables the provision of more terminations within a given component area and terminations with a much finer pitch.

A general object of the present technology is to provide termination features that enable an effective solder base with reduced susceptibility to solder leaching and also lowered insulation resistance. Configuration of exposed electrode portions and anchor tab portions is designed such that selected adjacent exposed tab portions are decorated with plated termination material without undesired bridging among distinct termination locations.

Yet another object of the present subject matter is that the disclosed technology can be utilized in accordance with a myriad of different termination configurations, including varied numbers and placement of external terminations. Plated terminations can be formed in accordance with a variety of different plating techniques as disclosed herein at locations that are self-determined by the provision of exposed conductive elements on the periphery of an electronic component.

A still further object of the subject plated termination technology is to facilitate the production of cheaper and more effective electronic components in an expedient and reliable manner.

Additional objects and advantages of the invention are set forth in, or will be apparent to those of ordinary skill in the art from, the detailed description herein. Also, it should be further appreciated by those of ordinary skill in the art that modifications and variations to the specifically illustrated, referenced, and discussed features hereof may be practiced in various embodiments and uses of the disclosed technology without departing from the spirit and scope thereof, by virtue of present reference thereto. Such variations may include, but are not limited to, substitution of equivalent means and features, or materials for those shown, referenced, or discussed, and the functional, operational, or positional reversal of various parts, features, or the like.

Still further, it is to be understood that different embodiments, as well as different presently preferred embodiments, of this invention may include various combinations or configurations of presently disclosed features or elements, or their equivalents (including combinations of features or configurations thereof not expressly shown in the figures or stated in the detailed description).

A first exemplary embodiment of the present subject matter relates to a multilayer electronic component with electrolessly plated terminations. Such a multilayer electronic component may preferably include a plurality of insulating substrates with a plurality of electrodes interleaved among the substrates. Each respective electrode preferably has at least one tab portion extending therefrom that is exposed along selected edges of the plurality of insulating substrates. Selected of the exposed

electrode tab portions are preferably stacked within a predetermined distance of one another such that a plurality of electrolessly plated terminations may be formed along the periphery of the electronic component. In some exemplary embodiments, the electrodes and respective tab portions may be provided in an interdigitated configuration with the electrode tab portions extending to, for example but not limited to, one, two, or four sides of the multilayer electronic component. In other exemplary embodiments, the electrodes may be provided in generally T-shaped and/or J-shaped configurations.

Another related embodiment of the disclosed technology concerns an electronic component such as the aforementioned first exemplary embodiment, further including additional anchor tabs. In such an exemplary embodiment, anchor tabs may also be interspersed among the plurality of substrate layers and exposed at predetermined locations such that the formation of plated terminations is guided by the location of the exposed electrode tab portions and the exposed anchor tabs. With the provision of a sufficient stack of exposed tabs as well as an exposed tab on at least one of the top and bottom surfaces of the body of dielectric material aligned with the stack of exposed tabs, the formation of a plated termination that extends along an entire exposed side and that wraps around one or both of the top and bottom surfaces of the electronic component is possible and usually, but not always, desirable. Resultant J-shaped or U-shaped terminations provide lands for facilitated mounting of the electronic component to a printed circuit board or other mounting location. Alternatively, exposed tabs that extend along an entire side without wrapping around to top and/or bottom surfaces may be formed by providing anchor tabs into respective corner radius portions of the device, thus facilitating a land-less termination that still enables good

solder wetting to a printed circuit board or other mounting surface.

In some exemplary embodiments of the present subject matter, terminations comprise one or more layers of plated termination material, on top of which are provided additional termination layers. One example of such a multilayer termination corresponds to an initial plated layer of copper followed by successive layers of nickel and tin, which may also be plated in accordance with presently disclosed methodologies.

Another exemplary embodiment of the present invention corresponds to a multilayer electronic component including respective pluralities of first and second ceramic layers, a plurality of electrodes, and at least one layer of plated termination material. The electrodes are selectively interleaved with the plurality of first ceramic layers to form an internal assembly, and the second ceramic layers are provided on opposing outer surfaces of the internal assembly to form cover layers for the electronic component. Electrically isolated anchor tabs may be optionally embedded among the first and/or second ceramic layers to further nucleate and guide the formation of the plated termination material.

Yet another exemplary embodiment of the present subject matter relates to an interdigitated capacitor comprising a plurality of interleaved electrode and dielectric layers and characterized by respective topmost and bottommost layers. The topmost and bottommost layers of the multilayer interdigitated capacitor preferably comprise dielectric cover layers with a thickness greater than that of the other dielectric layers in the stacked configuration. Each respective electrode layer includes a plurality of electrode tabs that extends to selected sides of the interdigitated capacitor. The electrode tabs are preferably exposed in stacked portions at selected locations

along the sides of a capacitor. Anchor tabs are preferably embedded within the top and bottom cover layers and optionally within the active layers such that an exposed stack of tabs extends along a portion of an entire side of the multilayer device. External terminations may then be plated along the stack of exposed tabs and may even wrap around to one or both of the topmost and bottommost layers if anchor tabs are positioned thereon and generally aligned with the stack of exposed internal tabs. Exposed tabs that extend along an entire side without wrapping around to the topmost and/or bottommost layers may include anchor tabs into respective corner radius portions of the top and bottom cover layers of the device, thus facilitating a land-less termination that still enables good solder wetting to a printed circuit board or other mounting surface.

The present subject matter equally concerns methodology associated with forming multilayer electronic components in accordance with the disclosed technology. One exemplary embodiment of such methodology includes the steps of providing a plurality of electronic components, providing an electroless bath solution, and immersing the electronic components in the electroless bath solution for a predetermined amount of time. The electronic components respectively include a plurality of ceramic substrate layers selectively interleaved with a plurality of internal electrodes. Selected portions of the internal electrodes are exposed at locations along the periphery of each electronic component such that immersion in the electroless bath solution enables a termination material to be deposited on the plurality of electronic components to form bridged terminations for the respective components.

An additional exemplary step in accordance with the present subject matter may include a step of cleaning selected surfaces of the electronic components, such as via chemical polishing,

before immersing the components in the electroless bath solution. A still further exemplary step corresponds to a step of applying an activation material to the exposed electrode portions, such as by immersion in metallic salts, photo-patterned organometallic precursors, screen-printed or ink-jetted Palladium deposition, and/or electrophoretic metallic deposition. Yet another exemplary step corresponds to a heating or annealing step to strengthen adhesion of the plated termination material to the electronic component.

Additional embodiments of the present subject matter, not necessarily expressed in this summarized section, may include and incorporate various combinations of aspects of features or parts referenced in the summarized objectives above, and/or features or parts as otherwise discussed in this application.

Those of ordinary skill in the art will better appreciate the features and aspects of such embodiments, and others, upon review of the remainder of the specification.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

A full and enabling description of the present subject matter, including the best mode thereof, directed to one of ordinary skill in the art, is set forth in the specification, which makes reference to the appended figures, in which:

Figure 1A illustrates a generally top exploded view of a known exemplary electrode layer configuration for a multilayer interdigitated capacitor;

Figure 1B illustrates a generally side perspective view of an exemplary multilayer interdigitated capacitor with an internal electrode layer configuration such as the known exemplary embodiment illustrated in Figure 1A;

Figure 2A illustrates a generally top exploded view of an exemplary internal electrode layer and anchor tab configuration

for a multilayer interdigitated capacitor in accordance with the present subject matter;

Figure 2B illustrates a generally side perspective view of an exemplary multilayer interdigitated capacitor in accordance with the present subject matter with internal electrode and anchor tab portions such as illustrated in Figure 2A;

Figure 3A illustrates a generally top exploded view of a known exemplary internal electrode layer configuration for a multilayer capacitor;

Figure 3B illustrates a generally top exploded view of an exemplary internal electrode layer and anchor tab configuration for a multilayer capacitor in accordance with the present subject matter;

Figure 4A illustrates a generally side perspective view of an exemplary multilayer capacitor in accordance with the present subject matter with internal electrode and anchor tab portions such as illustrated in Figure 3B;

Figure 4B illustrates a generally side perspective view of an exemplary multilayer interdigitated capacitor in accordance with the present subject matter, featuring internal electrode and anchor tab portions exposed on four selected sides of the exemplary capacitor configuration;

Figures 5A and 5B respectively illustrate generally top views of a known electrode layer configuration for use in exemplary multilayer capacitor embodiments;

Figure 5C illustrates a generally side perspective view of an exemplary multilayer capacitor embodiment with electrode layer configurations such as the known exemplary representations of Figures 5A and 5B;

Figures 6A and 6B respectively illustrate generally top views of an exemplary electrode layer configuration in

accordance with the present subject matter for use in multilayer capacitor embodiments;

Figure 6C illustrates a generally side perspective view of an exemplary multilayer capacitor embodiment in accordance with the present subject matter with electrode layer configurations such as those illustrated in Figures 6A and 6B;

Figure 7A illustrates a generally side perspective view of an exemplary capacitor array with exposed electrode tabs;

Figure 7B illustrates a generally side perspective view of an exemplary capacitor array with plated terminations in accordance with the present subject matter;

Figure 8A illustrates a generally side perspective view of an exemplary multilayer interdigitated capacitor with plated terminations in accordance with the present subject matter;

Figure 8B illustrates a side cross-sectional view of an exemplary multilayer interdigitated capacitor with exemplary plated terminations in accordance with the disclosed technology taken along planar section line A-A of Figure 8A;

Figure 9A illustrates a generally side view, with slight top perspective, of an exemplary monolithic integrated passive component with exposed electrode tabs and additional anchor tabs in accordance with the disclosed technology;

Figure 9B illustrates a generally side view, with slight top perspective, of an exemplary monolithic integrated passive component with plated terminations in accordance with the present subject matter;

Figure 10A illustrates a generally side cross-sectional view of an exemplary multilayer electronic component having electrodes and anchor tabs positioned and exposed for forming an "I-shaped" termination in accordance with the presently disclosed technology;

Figure 10B illustrates a generally side cross-sectional view of an exemplary multilayer electronic component with "I-shaped" terminations, such as formed via subjection of the embodiment depicted in Figure 10A to selected plating processes as presently disclosed in accordance with the present subject matter;

Figure 11A illustrates a generally side cross-sectional view of an exemplary multilayer electronic component having electrodes and anchor tabs positioned and exposed for forming a "J-shaped" termination in accordance with the presently disclosed technology;

Figure 11B illustrates a generally side cross-sectional view of an exemplary multilayer electronic component with "J-shaped" terminations, such as formed via subjection of the embodiment depicted in Figure 11A to selected plating processes as presently disclosed in accordance with the present subject matter;

Figure 12A illustrates a generally side cross-sectional view of an exemplary multilayer electronic component having electrodes and anchor tabs positioned and exposed for forming an "U-shaped" termination in accordance with the presently disclosed technology;

Figure 12B illustrates a generally side cross-sectional view of an exemplary multilayer electronic component with "U-shaped" terminations, such as formed via subjection of the embodiment depicted in Figure 12A to selected plating processes as presently disclosed in accordance with the present subject matter;

Figures 13A and 13B respectively illustrate generally top views of an exemplary electrode layer configuration in accordance with the present subject matter for use in multilayer capacitor embodiments;

Figure 13C illustrates a generally side perspective view of an exemplary multilayer capacitor embodiment in accordance with the present subject matter with electrode layer configurations such as those illustrated in Figures 13A and 13B;

Figures 14A and 14B respectively illustrate generally top views of an exemplary electrode layer configuration in accordance with the present subject matter for use in multilayer capacitor embodiments; and

Figure 14C illustrates a generally side perspective view of an exemplary multilayer capacitor embodiment in accordance with the present subject matter with electrode layer configurations such as those illustrated in Figures 14A and 14B.

Repeat use of reference characters throughout the present specification and appended drawings is intended to represent same or analogous features or elements of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

As referenced in the Brief Summary of the Invention section, the present subject matter is directed towards improved termination features for monolithic electronic components.

The subject termination scheme utilizes exposed electrode portions of structures such as monolithic capacitor arrays, multilayer capacitors including those with interdigitated electrode configurations, integrated passive components, and other electronic chip structures. Additional anchor tabs may be embedded within such monolithic components to provide stacked pluralities of exposed internal conductive portions to which plated terminations may be formed and securely positioned along the periphery of a device.

By providing additional anchor tabs on selected top and/or bottom surfaces of a chip device, wrap-around plated terminations may be formed that extend along the side of a chip to one or more of the top and bottom layers. Such wrap-around

terminations may be desirable in certain applications to facilitate soldering of the chip to a printed circuit board or other suitable substrate. Exposed tabs that extend along an entire side without wrapping around to the top and/or bottom layers may be formed by providing anchor tabs into respective corner radius portions of the top and bottom cover layers of the device, thus facilitating a land-less termination that still enables good solder wetting to a printed circuit board or other mounting surface.

The subject plating technology and anchor tab features may be utilized in accordance with a plurality of different monolithic components. Figures 1A and 1B represent aspects of known interdigitated electrode layer configurations wherein electrode tabs generally extend to and are exposed on two selected sides of a multilayer component. Aspects of plated terminations in accordance with the present subject matter are thereafter presented with respect to Figures 2A and 2B, which also concern multilayer component embodiments with exposed conductive portions of two selected sides of a device.

Figure 3A illustrates aspects of a known electrode layer configuration with electrode tabs for exposure on one selected side of a multilayer electronic device. Figures 3B and 4A, respectively, relate to improvements of the exemplary embodiment presented in Figure 3A, providing for an exemplary multilayer capacitor with internal electrode tabs exposed on one selected side of the capacitor and featuring anchor tabs in accordance with the present technology. Figure 4B relates to an exemplary multilayer interdigitated component with internal electrode tabs and anchor tabs exposed of four selected sides of the component in accordance with the present subject matter.

Still further exemplary embodiments of the present subject matter relate to the multilayer capacitor configurations

illustrated in Figures 6A through 6C, respectively, which are improvements to the exemplary multilayer capacitor configurations of Figures 5A through 5C, respectively. Additional examples of multilayer capacitor configurations are illustrated in Figures 13A through 13C and 14A through 14C, respectively. Still further embodiments of the disclosed technology are presented with reference to the exemplary capacitor arrays of Figure 7A and 7B. Figures 8A and 8B then represent aspects of the subject plated termination features, while Figures 9A and 9B concern an exemplary integrated passive component with selective terminations in accordance with the present subject matter. As more particular examples of possible uses of the presently disclosed technology, Figures 10A and 10B depict aspects of "I-shaped" terminations, while Figures 11A and 11B depict aspects of "J-shaped" terminations and Figures 12A and 12B depict aspects of "U-shaped" terminations.

It should be noted that each of the exemplary embodiments as presented herein should not insinuate limitations of the disclosed technology. Features illustrated or described as part of one embodiment can be used in combination with another embodiment to yield further embodiments. Additionally, certain features may be interchanged with similar devices or features not mentioned yet which perform the same, similar or equivalent function.

Reference will now be made in detail to the presently preferred embodiments of the disclosed technology. Referring to the drawings, Figure 1A illustrates a known exemplary configuration of electrode layers 10 and 12 with electrode tabs 14 for use in a multilayer interdigitated capacitor or capacitor array. Electrode layers are arranged in parallel with tabs 14 extending from the layers such that electrode tabs extending from alternating electrode layers 10 and 12 are aligned in

respective columns. The exemplary illustration depicts four such electrode layers with corresponding tabs 14, but typical arrangements as utilized with the present technology may in some instances contain many more electrode layers and respective tabs. This feature provides the option of creating capacitive elements with a large range of capacitance values (by choosing the number of electrodes).

The exemplary electrode layer configuration of Figure 1A is not representative of a finished capacitor embodiment. Instead, Figure 1A provides a reference for an intermediate aspect of exemplary capacitor and capacitor array configurations. The electrode layer configuration of Figure 1A can be utilized in accordance with an exemplary multilayer interdigitated capacitor such as displayed in Figure 1B.

An interdigitated capacitor typically consists of a plurality of electrode layers, such as those shown in Figure 1A disposed in a body of dielectric material 18, such as seen in the exemplary interdigitated capacitor configuration 16 of Figure 1B. Electrode layers 10 and 12 are disposed in the dielectric material 18 such that electrode tabs 14 extend to and are exposed at two sides of IDC embodiment 16. Exemplary materials for such electrode layers may include platinum, nickel, a palladium-silver alloy, or other suitable conductive substances. Dielectric material 18 may comprise barium titanate, zinc oxide, alumina with low-fire glass, or other suitable ceramic or glass-bonded materials. Alternatively, the dielectric may be an organic compound such as an epoxy (with or without ceramic mixed in, with or without fiberglass), popular as circuit board materials, or other plastics common as dielectrics. In these cases the conductor is usually a copper foil which is chemically etched to provide the patterns.

Exemplary IDC embodiment 16 may alternatively be viewed as a multilayer configuration of alternating electrode layers and dielectric layers in portion 20 of the device. IDC 16 is typically further characterized by a topmost dielectric layer 22 and bottommost dielectric layer 24 that may be built up to be generally thicker than other dielectric layer portions of IDC configuration 16. Such dielectric layers 22 and 24 act as cover layers to protect the device and provide sufficient bulk to withstand the stress of glass/metal frit that may be fired to a capacitor body. Known capacitor embodiments have utilized the multilayer arrangement of Figure 1B, and the present subject matter utilizes aspects of such configuration 16 in accordance with additional features disclosed herein.

A multilayer IDC component 16 such as that of Figure 1B that incorporates the known exemplary electrode layer configuration of Figure 1A is characterized by electrode portions 14 that are exposed on two selected sides of IDC component 16. Other exemplary internal electrode configurations may be employed in a multilayer component such that internal electrode portions are exposed at different locations and/or on different numbers of sides of the device.

For example, consider the exemplary internal electrode layer configuration illustrated in the exploded view of Figure 3A. Alternating electrode layers 26 and 28 are provided with electrode tab portions 30 extending toward a single selected direction. Electrode tabs 30 for each set of alternating electrode layers are preferably arranged in a stacked configuration such that, for instance, tabs 30 from electrode layers 26 are aligned in two respective columns. A similar alignment situation preferably holds for tabs 30 of electrode layers 28. A multilayer capacitor or other passive component that utilizes the exemplary internal electrode configuration of

Figure 3A will typically be configured such that electrode tab portions 30 are exposed on a single selected side of the component.

Yet another exemplary internal electrode layer configuration provides for electrode tabs that are exposed on four sides of a multilayer interdigitated component. Such internal electrode layers may be similar to the configuration depicted in Figure 1A wherein each alternating electrode layer 10 and 12 has additional tab portions on the sides of the layers adjacent to the sides from which tab portions 14 extend.

A still further exemplary electrode layer configuration and corresponding multilayer capacitor embodiment is depicted in Figures 5A through 5C, respectively. A first plurality of internal electrode layers 32 such as in Figure 5A are interleaved with internal electrode layers 34, such as in Figure 5B, in a body of dielectric material 36 to form a multilayer capacitor 38 such as in Figure 5C. In such exemplary multilayer component 38, portions 40 of one set of electrode layers 32 or 34 is exposed on side 42 of component 38. The portions of the other set of electrode layers 32 or 34 is thus exposed on the side of the device opposite of side 42 (not seen in the drawing).

Referring again to Figure 1B, a typical conventional termination for IDC embodiment 16 and for other monolithic electronic components comprises a printed and fired thick-film stripe of silver, copper, or other suitable metal in a glass matrix, on top of which is plated a layer of nickel to promote leach resistance, and is followed by a layer of tin or solder alloy which protects the nickel from oxidation, and promotes an easily soldered termination.

A thick-film stripe in accordance with such type of termination also typically requires printed application by a

termination machine and printing wheel or other suitable component to transfer a metal-loaded paste. Such printing hardware may have resolution limits that make it hard to apply thick-film stripes, especially to smaller chips. A typical existing size for an IDC 16 or other electronic component is about one hundred and twenty mils (thousandths of an inch) by sixty mils along the two opposing sets of sides with a thickness from top to bottom layers of about thirty mils. When more than four terminations need to be applied to a part this size or terminations are desired for a part with smaller dimensions, the resolution levels of specialized termination machinery often becomes a limitation in applying effective termination stripes.

The present subject matter offers a termination scheme that eliminates or greatly simplifies the provision of such typical thick-film termination stripes. By eliminating the less-controlled thick film stripe, the need for typical termination printing hardware is obviated. Termination features in accordance with the disclosed technology focus more on the plated layer of nickel, tin, copper, etc. that is typically formed over a thick-film termination stripe.

With plated terminations in accordance with the presently disclosed technology, it should be appreciated that it is possible to form terminations that are the same width along a component's periphery as that of the exposed internal electrodes. In prior art termination schemes, where thick-film termination stripes are applied, the terminations are typically wider than the exposed electrode portions to account for potential misregistration of exposed tabs. Exposed electrode portions in such prior art embodiments must typically be narrow enough to not only ensure complete coverage thereof by the terminations, but also to ensure that adjacent terminations do not short together. In accordance with aspects of the presently

disclosed plated terminations, maximizing the width of internal electrode tabs yields electronic components with advantageously lower equivalent series inductance (ESL).

Consider the exemplary capacitor array configuration 44 presented in Figure 7A. Capacitor array 44 is characterized by a plurality of internal electrodes and corresponding electrode tabs 46 embedded in a body of dielectric material 48. As opposed to the electrode layers of exemplary IDC configuration 16, the electrode tabs 46 of capacitor array 44 typically correspond to separate internal electrodes. By subjecting capacitor array 44 or other electronic component with similarly exposed electrode tabs to an electroless plating solution, for example nickel or copper ionic solution, the formation of plated terminations 50, such as is shown in Figure 7B, is preferably effected. Exposure to such solution enables the exposed electrode tabs 46 to become deposited with nickel, copper, tin or other metallic plating. The resulting deposition of plated material is preferably enough to effect an electrical connection between adjacent electrode tabs 46 in a stacked column. The distance between adjacent electrode tabs in a column of tabs should preferably be no greater than about ten microns to ensure proper plating. The distance between adjacent columnar stacks of electrode tabs 46 should thus be greater by at least a factor of 2 than this minimum distance to ensure that distinct terminations 50 do not run together. In some embodiments of the present technology, the distance between adjacent columnar stacks of exposed metallization is about four times the distance between adjacent exposed electrode tabs 46 in a particular stack. By controlling the distance between exposed internal conductor portions, termination connectivity can be manipulated to form bridged or non-bridged terminations depending on the desired termination configuration.

Plated terminations 50 are thus guided by the positioning of the exposed electrode tabs 46. This phenomena is hereafter referred to as "self-determining" since the formation of plated terminations 50 is determined by the configuration of exposed metallization at selected peripheral locations on multilayer component, or capacitor array, 44. The exposed internal electrode tabs 46 also help anchor terminations 50 to the periphery of capacitor array 44', which corresponds to a multilayer capacitor embodiment such as 44 of Figure 7A with the addition of plated terminations 50. Further assurance of complete plating coverage and bonding of the metals may be achieved by including resistance-reducing additives in the plating solution. A still further mechanism for enhancing the adhesion of metallic deposit that forms the subject plated terminations is to thereafter heat the component in accordance with such technologies as baking, laser subjection, UV exposure, microwave exposure, arcwelding, etc.

The plated terminations 50 of Figure 7B may be sufficiently formed for some component applications, but sometimes the exposed metallization from internal electrode tabs is insufficient to form the self-determining terminations of the present technology. In such case, it may be beneficial, and in some cases necessary, to provide additional anchor tabs embedded within select portions of a monolithic component. Anchor tabs are short conductive tabs that typically offer no electrical functionality to a component, but mechanically nucleate and secure additional plated termination along the periphery of a monolithic device. Exposed anchor tabs in combination with exposed internal electrode portions can provide sufficient exposed metallization to create more effective self-determining terminations.

For instance, consider the exploded configuration of exemplary internal metallization illustrated in Figure 2A. Alternating electrode layers 52 and 54 are provided in a similar configuration to the electrode layers of Figure 1A, with electrode tab portions 56 extending from selected locations of electrode layers 52 and 54. Additional anchor tabs 58 are also preferably provided in the same plane as active electrode layers 52 and 54 such that they are also exposed at selected locations along a multilayer component, yet offer no internal electrical connections. Additional anchor tabs may also be provided in the cover layers of a multilayer component and exposed along selected sides such that the formation of self-determining plated terminations that extend along even more of the component periphery is enabled.

With reference to Figure 2B, multilayer component 60 corresponds to an exemplary multilayer capacitor embodiment in accordance with the present subject matter. Portion 62 of multilayer component 60 preferably comprises the exemplary interdigitated electrode layer and anchor tab configuration of Figure 2A embedded within a portion of dielectric material. Solid lines 56 along the periphery of portion 62 are intended to represent exposed portions of the electrode tabs 56 of Figure 2A, and dashed lines 58 along the periphery of portion 62 represent exposed anchor tabs 58. Additional anchor tabs (not illustrated in Figure 2A) may be embedded within dielectric cover layers 64 and 66 (exposed portions of which are represented by dashed lines 68) to further provide an arrangement of exposed metallization for facilitating the formation of self-determining plated terminations in accordance with the present subject matter.

Internal anchor tabs are preferably aligned in a generally similar column as a stack of internal electrode tabs such that all internal tabs are arranged in common stacks.

For some component applications, it may be preferred that terminations not only extend along the entire width of a component, but also wrap around to the top and bottom layers. In this case, external anchor tabs 70 may be positioned on top and bottom layers of multilayer IDC 60 such that plated terminations can form along the sides and on portions of the top and bottom layers, forming extended solder lands. For example, the provision of embedded internal anchor tabs 58 and 68 and external anchor tabs 70 along with existing exposed electrode tabs 56 in IDC 60, such as depicted in Figure 2B, would facilitate the formation of wrap-around plated terminations 72, such as in Figure 8A.

There are several different techniques that can potentially be used to form plated terminations, such as terminations 72 on multilayer component embodiment 74 of Figure 8A. As previously addressed, a first method corresponds to electroplating or electrochemical deposition, wherein an electronic component with exposed conductive portions is exposed to a plating solution such as electrolytic nickel or electrolytic tin characterized by an electrical bias. The component itself is then biased to a polarity opposite that of the plating solution, and conductive elements in the plating solution are attracted to the exposed metallization of the component. Such a plating technique with **no** polar biasing is referred to as electroless plating, and can be employed in conjunction with electroless plating solutions such as nickel or copper ionic solution.

In accordance with electroless plating techniques, also referred to in some applications as immersion plating, preliminary steps may sometimes be utilized before immersing an

electronic component in a given electroless plating solution. After an electronic component is formed with exposed metallic electrode and/or anchor tab portions, a chemical polishing step may be effected to aid exposure of the metallic portions. For example, when electrode and/or anchor tab portions are made of Nickel, chemical polishing can help to chemically remove any buildup of Nickel Oxide (NiO) on the periphery of the yet unterminated component.

A still further example of a preliminary step that may be utilized in accordance with presently disclosed electroless plating techniques is a step to activate the exposed metallic portions of the device to facilitate depositing of the electrolessly plated materials. Activation can be achieved by immersion of the electronic component in Palladium salts, photo patterned Palladium organometallic precursors (via mask or laser), screen printed or ink-jet deposited Palladium compounds or electrophoretic Palladium deposition. It should be appreciated that Palladium-based activation is presently disclosed merely as an example of activation solutions that often work well with activation for exposed electrode and/or tab portions formed of Nickel or Nickel-based alloys. In other embodiments, alternative activation solutions may be utilized. In still further embodiments, a Palladium (Pd) dopant may be introduced into the Nickel ink that forms the capacitor electrodes to eliminate the Pd activation step for electroless Cu deposition. It should be further appreciated that some of the above activation methods, such as organometallic precursors, also lend themselves to co-deposition of glass formers for increased adhesion to the generally ceramic body of an electronic component.

In accordance with electrochemical deposition and electroless plating techniques, a component such as IDC 74 of

Figure 8A, is preferably submersed in an appropriate plating solution for a particular amount of time. With certain embodiments of the present subject matter, no longer than fifteen minutes is required for enough plating material to deposit at exposed conductive locations along a component such that buildup is enough to spread the plating material in a perpendicular direction to the exposed conductive locations and create a bridged connection among selected adjacent exposed conductive portions.

Another technique that may be utilized in accordance with the formation of the subject plated terminations involves magnetic attraction of plating material. For instance, nickel particles suspended in a bath solution can be attracted to similarly conductive exposed electrode tabs and anchor tabs of a multilayer component by taking advantage of the magnetic properties of nickel. Other materials with similar magnetic properties may be employed in the formation of plated terminations.

A still further technique regarding the application of plated termination material to exposed electrode tabs and anchor tabs of a multilayer component involves the principles of electrophoretics or electrostatics. In accordance with such exemplary technology, a bath solution contains electrostatically charged particles. An IDC or other multilayer component with exposed conductive portions may then be biased with an opposite charge and subjected to the bath solution such that the charged particles are deposited at select locations on the component. This technique is particularly useful in the application of glass and other semiconductive or nonconductive materials. Once such materials are deposited, it is possible to thereafter convert the deposited materials to conductive materials by intermediate application of sufficient heat to the component.

A related advantage of most of the methods disclosed herein for forming plated terminations is that multiple electronic components can be terminated in a bulk process, such as a barrel plating or fluidized bed termination processes. Such aspect facilitates more convenient and expedient component termination since device manufacture no longer requires the selective application of terminations via precisely configured termination machines.

It should also be appreciated that as these electronic parts get ever smaller, the practical matter of being able to physically hold them while applying the thick film termination to each end becomes less practicable.

Further, this thin film approach provides less dimensional variability, permitting easier automatic handling.

One particular methodology for forming plated terminations in accordance with the disclosed technology relates to a combination of the above-referenced plating application techniques. A multilayer component may first be submersed in an electroless plating solution, such as copper ionic solution, to deposit an initial layer of copper over exposed tab portions, and provide a larger contact area. The plating technique may then be switched to an electrochemical plating system which allows for a faster buildup of copper on the selected portions of such component.

In accordance with the different available techniques for plating material to exposed metallization of a multilayer component in accordance with the present technology, different types of materials may be used to create the plated terminations and form electrical connections to internal features of an electrical component. For instance, metallic conductors such as nickel, copper, tin, etc. may be utilized as well as suitable

resistive conductors or semi-conductive materials, and/or combinations of selected of these different types of materials.

A particular example of plated terminations in accordance with the present subject matter wherein plated terminations comprise a plurality of different materials is discussed with reference to Figure 8B. Figure 8B provides a cross-sectional view of component 74 of Figure 8A taken along planar section line A-A in accordance with a particular exemplary embodiment of plated terminations 72. It should be appreciated that terminations 72 may comprise only a first plating layer and no additional layers as presented in this example. Due to such potential for variation in the number of plating layers in the multilayer component and termination embodiments of Figures 8A and 8B, the two respective embodiments are labeled as 74 and 74' respectively, and such reference is not intended to insinuate additional variations between the two respective embodiments.

A first step in the formation of the terminations illustrated in Figure 8B involves submersing a component in an electroless plating solution, such as nickel or copper ionic solution, such that a layer of copper 76 or other metal is deposited along the periphery of component 74' where portions of internal anchor tabs 58 and 68, exposed internal electrode tabs extending from electrode layers 52 and 54, and external anchor tabs 70 are exposed. The tab area covered with metallic plating 76 can then be covered with a resistor-polymeric material 78 and then plated again with metallic copper or other material 80. In other exemplary embodiments, termination layer 78 may correspond to a solder barrier layer, for example a Ni-solder barrier layer. In some embodiments, layer 78 may be formed by plating an additional layer of nickel on top of the initial plated layer 76 (e.g., plated copper). A third exemplary termination layer 80 may in some embodiments correspond to a conductive layer,

such as plated Ni, Ni/Cr, Ag, Pd, Sn, Pb/Sn or other suitable plated solder.

A still further plating alternative corresponds to forming a layer of metallic plating, and then electroplating a resistive alloy over such metallic plating. Plating layers can be provided alone or in combination to provide a variety of different plated termination configurations. A fundamental of such plated terminations is that the self-determining plating is configured by the design and positioning of exposed conductive portions along the periphery of a component. It should be appreciated that the aforementioned plated terminations having multiple layers are not limited to utilization with the embodiments illustrated in Figures 8A and 8B, and may be practiced in accordance with all illustrated, disclosed and otherwise obvious electronic component variations.

Such particular orientation of internal electrode portions and anchor tabs may be provided in a variety of different configurations to facilitate the formation of plated terminations in accordance with the present subject matter. For instance, consider the exemplary internal conductive configuration of Figure 3B with electrode layers 26 and 28. Electrode tabs 30 and internal anchor tabs 82 may be provided in a body of dielectric material to create a multilayer component similar to that of Figure 4A. Additional internal anchor tabs 84 and external anchor tabs 86 may also be provided. One of the prescribed plating techniques may then be utilized to form plated terminations on multilayer component 88 along the exposed areas of metallization.

Yet another exemplary multilayer component in accordance with aspects of the present subject matter is represented as component 90 in Figure 4B. Internal electrode layers are provided with electrode tabs that extend to four sides of

component 90. Additional internal anchor tabs 94 may be interleaved with exposed electrode tabs 92. Still further internal anchor tabs 96 may be embedded within cover layers of component 90 to provide for expanded plated terminations. The provision of external anchor tabs 98 could facilitate the formation of wrap-around plated terminations to top and/or bottom sides of the component. Such external anchor tabs 98 may be printed directly into the ceramic plate or tape forming the topmost substrate layer to form an "embedded" layer that is completely flush with the topmost substrate layer. By embedding such portions of the electronic component, terminations may be less susceptible to partial breakage or inadvertent removal and a more aesthetically designed overall component may also be effected.

Examples of different peripheral termination shapes, such as effected by selective arrangement of external anchor tabs, are now presented with reference to Figures 10A, 10B, 11A, 11B, 12A and 12C. Referring more particularly to Figure 10A, a multilayer electronic component 150 has multiple pairs of opposing electrodes embodied by respective first electrodes 152 and respective second electrodes 154. Each electrode layer is formed on a respective ceramic layer, on which at least one anchor tab 156 may also be provided. Additional anchor tabs 158 may also be provided in dielectric cover layers without electrode elements, such that exposed conductive regions are provided along the general entirety of either side of multilayer component 150. By providing the exposed conductive anchor tabs 158 into the cover layers and approaching selected respective corners 157 of the component 150, the formation of generally "I-shaped" terminations 159a and 159b, such as depicted in Figure 10B is facilitated. Such "I-shaped" terminations provide a land-less termination that still enables good solder wetting to

a printed circuit board or other mounting surface, since the terminations preferably extend completely to the top and/or bottom surfaces of component 150.

Referring now to Figures 11A and 11B, a multilayer electronic component 160 has multiple pairs of opposing electrodes embodied by respective first electrodes 162 and respective second electrodes 164. Each electrode layer is formed on a respective ceramic layer, on which at least one anchor tab 166 may also be provided. Additional anchor tabs 168 may also be provided in dielectric cover layers without electrode elements, such that exposed conductive regions are provided along the general entirety of either side of multilayer component 160. External anchor tabs 165 are also preferably provided on a selected one of the top and bottom sides of component 160 such that resultant "J-shaped" terminations 169a and 169b are formed in accordance with the subject plating technology. Such "J-shaped" terminations provide lands for mounting the electronic component to a printed circuit board or other mounting surface, and since the lands are only on a selected side of component 108, a predetermined component mounting orientation is provided.

The absence of conductive portions on the top surface is sometimes desirable, for example, when the surface may come in contact with a heat shield or RF shield, which could cause a short circuit.

Referring now to Figures 12A and 12B, a multilayer electronic component 170 has multiple pairs of opposing electrodes embodied by respective first electrodes 172 and respective second electrodes 174. Each electrode layer is formed on a respective ceramic layer, on which at least one anchor tab 176 may also be provided. Additional anchor tabs 178 may also be provided in dielectric cover layers without

electrode elements, such that exposed conductive regions are provided along the general entirety of either side of multilayer component 170. External anchor tabs 175 are also preferably provided on both top and bottom sides of component 170 such that resultant "U-shaped" terminations 179a and 179b are formed in accordance with the subject plating technology. Such "U-shaped" terminations provide lands for mounting either side of electronic component 170 to a printed circuit board or other mounting surface.

With regard to Figures 10B, 11B and 12B, it should be appreciated that the respective terminations 159a, 159b, 169a, 169b, 179a and 179b may be selectively formed as single layer terminations or as multilayer terminations. For example, each peripheral termination in Figures 10B, 11B and 12B may correspond to a single layer of plated copper or nickel. Alternatively, such terminations may be formed to have an initial layer of plated copper followed by respective plated solder barrier and solder layers, for example nickel and then tin. In accordance with multilayered terminations, selected of the layers could be formed of a resistive or a semiconductive material.

A still further application of the presently disclosed technology relates to more general multilayer component configurations, such as depicted in Figures 6A, 6B and 6C. Electrode layer 100 of Figure 6A and electrode layer 102 of Figure 6B are provided in respective T-shaped configurations such that electrode tab portions 104 extend from the respective electrode layers. When electrode layers 100 and 102 are interleaved with dielectric layers to form a multilayer ceramic device, such as shown in Figure 6C, each electrode tab portion 104 is exposed on two adjacent sides of the device 108. Anchor tab portions 106 may also be provided within the electrode layer

planes such that exposed conductive portions are aligned along the opposing peripheral sides of device 108, to facilitate formation of plated electrodes thereon. After subjecting device 108 to one of the plating techniques described herein, the formation of corner terminations would be effected. It should be appreciated that provision of such terminations around selected corners of a multilayer electronic component was often difficult to achieve with prior art termination processes. It should be further appreciated by one of ordinary skill in the art that corner-terminated designs can be achieved not only in device 108, but in many other specifically configured devices, and it should further be appreciated that, analogous to the anchor tab discussion above, the corner wrap can be provided on only one corner, when that is desirable, as when an orientation feature may be needed.

Yet another example of a multilayer electronic component with which the presently disclosed technology may be utilized is depicted in Figures 13A, 13B and 13C. Electrode layer 130 of Figure 13A and electrode layer 132 of Figure 13B are provided in respective J-shaped configurations such that electrode tab portions 134 extend from the respective electrode layers. When electrode layers 130 and 132 are interleaved with dielectric layers and stacked to form a multilayer ceramic device, such as shown in Figure 13C, each electrode tab portion 134 (represented by an respective solid line) is exposed at selected locations along the top side of the device 138. Anchor tab portions 136 may also be provided within the electrode layer planes and/or within dielectric cover layers such that additional exposed conductive portions (as depicted by the respective dashed lines in Figure 13C) may facilitate formation of plated electrodes thereon. Components that utilize "J-shaped" electrodes as depicted in Figures 13A-13C have the advantage in certain

applications of having inherently predetermined component orientation, since terminations are formed only on one side of the component.

A slight variation to the "J-shaped" electrodes illustrated in Figures 13A-13C, respectively, corresponds to the "T-shaped" electrodes embodied in Figures 14A, 14B and 14C. Electrode layer 140 of Figure 14A and electrode layer 142 of Figure 14B are provided in respective T-shaped configurations such that electrode tab portions 144 extend from the respective electrode layers. When electrode layers 130 and 132 are interleaved with dielectric layers and stacked to form a multilayer ceramic device, such as shown in Figure 14C, each electrode tab portion 144 (represented by an respective solid line) is exposed at selected locations along both top and bottom sides of the device 148. Anchor tab portions 146 may also be provided within the electrode layer planes and/or within dielectric cover layers such that additional exposed conductive portions (as depicted by the respective dashed lines in Figure 14C) may facilitate formation of plated electrodes thereon.

Another example embodying aspects of the disclosed technology is presented with respect to Figures 9A and 9B. Figure 9A represents an integrated passive component 110, comprising a combination of passive components provided in a single monolithic structure. Integrated component 110 may include a selected combination of resistors, varistors, capacitors, inductors, couplers, baluns, and/or other passive components. Each distinct passive component is typically characterized by at least one conductive electrode-like portion from which at least one electrode tab portion 112 extends and is exposed along the periphery of component 110.

An integrated passive component 110, such as that represented by Figure 9A, may have a plurality of different

internal electrode arrangements as shown. Corresponding electrode tabs 112 may be provided in symmetrical or nonsymmetrical configurations and may be grouped in a variety of fashions. An important feature is that exposed electrode tabs 112 may be arranged within component 110 to facilitate the formation of selective plated terminations. In addition, internal anchor tabs 114 and/or external anchor tabs 116 may also be provided with an integrated passive component to create additional selective termination arrangements. For example, consider the exposed tab arrangement of Figure 9A, with numerous exposed internal electrode tabs 112, internal anchor tabs 114, and external anchor tabs 116. Subjecting such configuration to a plating solution in accordance with variations of the presently disclosed technology would preferably effect the formation of a plurality of plated side terminations 118 and plated wrap-around terminations 120, such as in Figure 9B. Integrated passive component, or multilayer electronics device, 110' simply corresponds to an integrated passive component such as 110 of Figure 9A with the addition of plated terminations 118 and 120, respectively. Thus, tabs of an integrated passive component can be designed whereby plated terminations can be formed among different electrodes and different component layers.

It should be appreciated that the monolithic component embodiments presented in Figures 1A through 9B, respectively, are presented merely as examples of the disclosed technology, including intermediate aspects thereof. In most of the examples, four or more general columns of electrodes are depicted, but a fewer or greater number of electrode columns are possible, depending on the desired component configuration. It is possible to form plated terminations along any selected portion of any selected component side in accordance with the

disclosed technology. Such plated terminations may include a single layer of plated conductive material, resistive material, or semi-conductive material, or a multilayer combination of selected of such materials.

It should be appreciated that internal anchor tabs and external anchor tabs may selectively be used for different termination preferences to provide different sizes of side terminations or wrap-around terminations. IDC embodiments displayed and described herein that feature both internal and external anchor tabs may, for instance, only utilize internal anchor tab features when wrap-around terminations are not preferred for a particular application. Different combinations of both internal and external anchor tabs with existing exposed electrode tabs on a variety of different multilayer components can yield numerous potential termination schemes for a device.

While the present subject matter has been described in detail with respect to specific embodiments thereof, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing may readily adapt the present technology for alterations to, variations of, and equivalents to such embodiments. Accordingly, the scope of the present disclosure is by way of example rather than by way of limitation, and the subject disclosure does not preclude inclusion of such modifications, variations, and/or additions to the present subject matter as would be readily apparent to one of ordinary skill in the art.